ABSTRACT:

Semiconductor device comprising an integrated CMOS circuit with NMOS and PMOS transistors (A, B) having semiconductor zones (23, 24, 29, 30) formed in a silicon substrate (1). At the locations of the gate zones (29, 30), the surface (3) of the substrate is provided with a layer of gate oxide (11) on which gate electrodes (16, 17) are formed. The gate electrodes (17) of the PMOS transistors (B) are formed in a layer of p-type doped polycrystalline silicon (14) and a layer of p-type doped polycrystalline silicon-germanium(13) ($Si_{1-x}Ge_x$; $0 < x < 1$) sandwiched between the silicon-germanium layer and the gate oxide. The gate electrodes (16) of the NMOS transistors (A) are formed in a layer of n-type doped polycrystalline silicon (14) without germanium. The integrated CMOS circuit combines advantages of PMOS transistors having p-type doped silicon-germanium gate electrodes with advantages of NMOS transistors having n-type doped silicon gate electrodes.

Fig. 13